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Review on Reducing the Power in Network-on-chip

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Abstract

Network-on-chip(NoC) is an emerging revolutionary method to integrate numerous cores in a single System-on-Chip (SoC). The network-on-chip (NoC) design paradigm is recognized as the most viable way to tackle with scalability and variability issues that characterize the ultradeep submicronmeter era. A significant fraction of the overall power dissipation of a network-on-chip (NoC) based system-on-chip (SoC) is due to the interconnection system. The advancements in the future technology makes it possible to place larger number of transistors on a single die, together with many different layers of interconnect and their contribution is expected to increase and compete with the power dissipated by the other elements of the communication subsystem, namely, the routers and the network interfaces (NIs). In this paper, we surveyed recent data encoding techniques aimed at reducing the power dissipated by the network links.

Keywords:Coupling switching activity, data encoding, interconnection on chip, low power, network-on-chip, power analysis

Introduction

As the number of cores integrated into a system-on-chip (SoC) increases the interconnection system becomes more and more important. International roadmap for semiconductors depicts the on-chip communication issues as the limiting factors for performance and power consumption in current and next generation SoCs. Shifting from a silicon technology node to the next one resulted in faster and more power efficient gates but slower and more power hungry wires. In fact, more than 50% of the total dynamic power is dissipated in interconnects in current processors, and this is expected to rise to 65%–80% over the next several years. Global interconnect length does not scale with smaller transistors and local wires it increases at a very high rate even though gate delay and lower level metal interconnect delay are decreasing. Chip size remains relatively constant because the chip function continues to increase and RC delay increases exponentially.

Now-a-days, the on-chip communication issues are as relevant as, and in some cases more relevant than, the computation related issues. In fact, the communication subsystem increasingly impacts the traditional design objectives, including cost (i.e., silicon area), performance, power dissipation, energy consumption, reliability, etc. As technology shrinks, an ever more significant fraction of the total power budget of a complex many-core system-on-chip (SoC) is due to the communication subsystem. The power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales. SoC consisting of tens of cores were common in the last decade, common predictions shows that the next generation of many-cores SoC will contain hundreds or thousands of cores. A significant fraction of the total system power budget is dissipated by interconnection networks. The basic elements which form a NoC based interconnect are network interfaces (NIs), routers, and links. As technology shrinks, the power dissipated by the links is as relevant as (or more relevant than) that dissipated by routers and NIs

Related works

Agarwal *et al* [1] In the upcoming years, the availability of chips with 1000 cores might be seen. In these chips, the total system power budget has a significant fraction of dissipation only by interconnection networks. Hence,the design of power-efficient interconnection networks has been the focus of many works in the literature dealing with

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NoC architectures. These works concentrate on different components of the interconnection networks such as routers, Network interface and links.The focus of this paper is on reducing the power dissipated by the links, some works in reducing the power is surveyed below. These include the techniques that make use of passive shielding which is used to reduce the capacitive coupling effects of adjacent bus lines by inserting passive ground or power lines between them. Active shielding another technique which switches depending on the switching pattern of its adjacent bus lines [2], usage of nonuniform wire spacing savings of up to 40% was obtained at no complexity or performance cost [3],and repeater insertion. These all leads to increase in the chip area. An another method is the data encoding scheme that was employed to reduce the link power dissipation. The data encoding techniques may be classified into two categories. In the first category is given by encoding techniques which concentrates on lowering the power caused by self-switching activity of individual bus lines by reducing the power dissipation owing to their coupling switching activity. In this category, the type of coding used is Bus-Invert (BI) method of coding.
Stan *et al.* [4] presented Bus-Invert method of coding which helps in lowering the I/O bus activity and thus decreases the I/O peak power dissipation by 50% and the I/O average power dissipation is upto 25%[4]. This decreases the performance when tradeoff is made between performance and power dissipation.The number of transitions from 0 to 1 for two consecutive flits (the flit that just traversed and the one which is about to traverse the link) is counted. If the number is larger than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred via the link. This technique is only concerned about the self-switching without worrying the coupling switching. Note that the coupling capacitance in the state-of–the-art silicon technology is considerably larger (e.g., four times) compared with the self-capacitance. In addition, the scheme was based on the hop-by-hop technique, and therefore, encoding/decoding is performed in each node.

Ramprasad *et al.* [5] a source coding framework is presented which describes encoding schemes to reduce transition activity. The INC-XOR scheme proposed for the random data patterns are transmitted through these lines which reduces the number of transitions by assigning fewer transitions to the more frequently occurring set of transitions in the original signal. It is based on obtaining a prediction function and a prediction error. This prediction error is XORed with the previous value sent to the bus so that the number of transitions is reduced. Gray[6] and T0 [7] encoding are targeted to situations in which consecutive accesses differ by one (or by a fixed stride). The Gray encoding is useful because the encoding of these values differs by one bit. In the T0 encoding an additional wire is used to indicate the consecutive access mode, and no activity is required in the bus.

Musoll *et al.* [8] Working zone encoding (WZE) presents a method for encoding an external address bus. without instruction and data caches, this scheme is beneficial for data address and shared buses, cases which that have the largest number of bus transitions and for which other coding are less effective. The major drawback of the WZE is its larger encoder and decoder logic overhead, which limits the benefits of the I/O activity reduction

Jantsch *et al.* [9] analyzed the use of partial bus invert coding as link level low power encoding technique with the conclusion that it spends several times more power than no encoding at all, if normalized for the same performance, which is done by adjusting supply voltage and frequency. However, differently from how we propose in this paper, they considered point-to-point encoding in which every router in the NoC decodes the incoming flits and encodes the outgoing flits. In addition, [9] did not take advantage of the pipelined nature of the wormhole switching.

This category of encoding techniques is not suitable to be applied in the deep submicronmeter technology nodes where the coupling capacitance constitutes a major part of the total interconnect capacitance. This causes the power consumption due to the coupling switching activity to become a large fraction of the total link power consumption. A coding technique that reduces the coupling switching activity by taking the advantage of end-to-end encoding for wormhole switching has been presented in [10]. It is based on lowering the coupling switching activity by eliminating only Type II transitions. The power and energy saving due to the reduction of the switching activity in network links, but also the overhead (both in terms of power dissipation and silicon area) due to the encoding and decoding logic integrated into the NI showed that up to 37% of power dissipation and up to 18% of energy consumption can be saved.
The techniques proposed in [11] and [12] have a smaller number of control lines but the complexity of their decoding logic is high. The technique described

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in [11] is as follows: first, the data are both odd inverted and even inverted, and then transmission is performed using the kind of inversion which reduces more the switching activity. In [12], the coupling switching activity is reduced up to 39%. In this paper, compared to [12], a simpler decoder while achieving a higher activity reduction.

Kwang *et al* [13] Coupling effects between on-chip interconnects must be addressed in ultra deep submicron VLSI and system-on-a-chip (SoC) designs. A new low-power bus encoding scheme is proposed to minimize coupled switching which dominate the on-chip bus power consumption. The coupling-driven bus invert method use slim encoder and decoder architecture to minimize the hardware overhead. Experimental results indicate that our encoding methods save effective switching as much as 30% in an 8-bit bus with one-cycle redundancy.The scheme presented in [13] dealt with reducing the coupling switching. In this method, a complex encoder counts the number of Type I transitions with a weighting coefficient of one and the number of Type II transitions with the weighting coefficient of two. If the number is larger than half of the link width, the inversion will be performed. In addition to the complex encoder, the technique only works on the patterns whose full inversion leads to the link power reduction while not considering the patterns whose full inversions may lead to higher link power consumption. Therefore, the link power reduction achieved through this technique is not as large as it could be. This scheme was also based on the hop-by-hop technique.

Pande *et al.* [14] proposed the use of crosstalk avoidance codes (CAC) to improve the signal integrity by reducing the effective coupling capacitance and lowering the energy dissipation of wire segments [14]. By incorporating CAC in NoC data streams the effective coupling capacitance of the inter-switch wire segments and hence the communication energy is reduced without incurring the non-optimal wire area overhead of shielding/spacing. However, its application requires redundant wires and the encoding/decoding process is performed hop by hop for the header flit In another coding technique presented in [14], bunches of four bits are encoded with five bits. The encoded bits were isolated using shielding wires such that the occurrence of the patterns “101” and “010” were prevented. This way, no simultaneous Type II transitions in two adjacent pair bits are induced. This technique effectively reduces the coupling switching activity. Although the technique reduces the power consumption considerably, it increases the data transfer time, and hence, the link energy consumption. This is due to the fact that for each four bits, six bits are transmitted which increases the communication traffic. This technique was also based on the hop-by-hop approach.

Khademzadeh *et al.*[15] presented a set of three data encoding schemes aimed at reducing the power dissipated by the links of an NoC. In Scheme I, it is focused on reducing Type I transitions while in Scheme II, both Types I and II transitions are taken into account for deciding between half and full invert, depending the amount of switching reduction. Finally, in Scheme III, the Type I transitions showed different behaviours in the case of odd and even inverts and makes the inversion which leads to the higher power saving. The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimizing the self-switching activity and the coupling switching activity in the links traversed by the flits. In this end-to-end encoding technique takes advantage of the pipeline nature of the wormhole switching technique. An encoder and a decoder block are added to the NI. Except for the header flit, the encoder encodes the outgoing flits of the packet such that the power dissipated by the inter-router point-to-point link is minimized.

Conclusion

In this report, we have surveyed the different encoding schemes for reducing the power dissipated by the links of a NoC. These schemes have several drawbacks as discussed above and this category of encoding is not suitable to be applied in the deep submicronmeter technology nodes, their contribution is expected to increase in future technology nodes. Compared to the previous encoding schemes proposed in the literature, the final three set of encoding scheme is to minimize not only the switching activity, but also the coupling switching activity which is mainly responsible for link power dissipation in the deep submicronmeter technology regime.

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